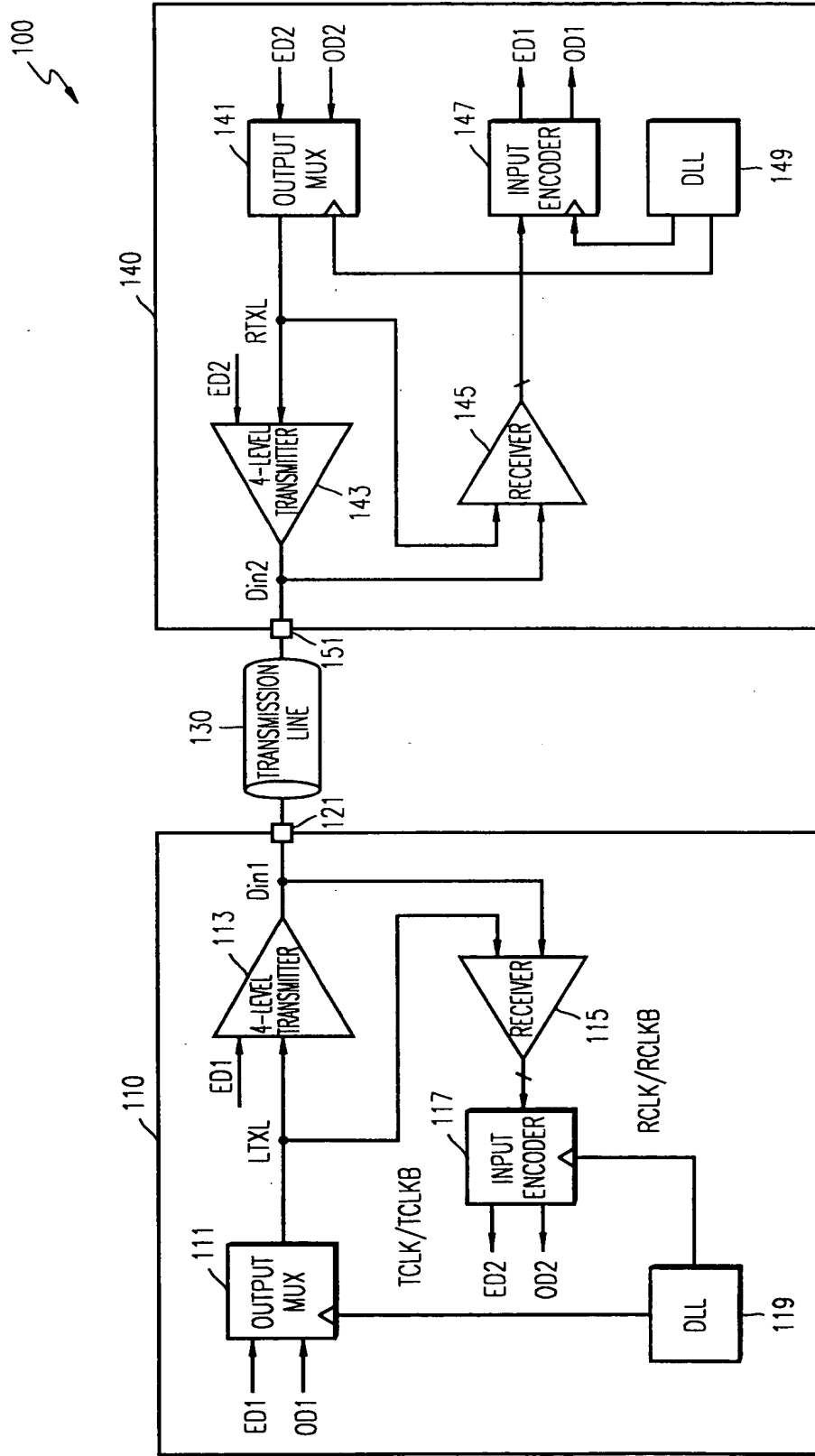
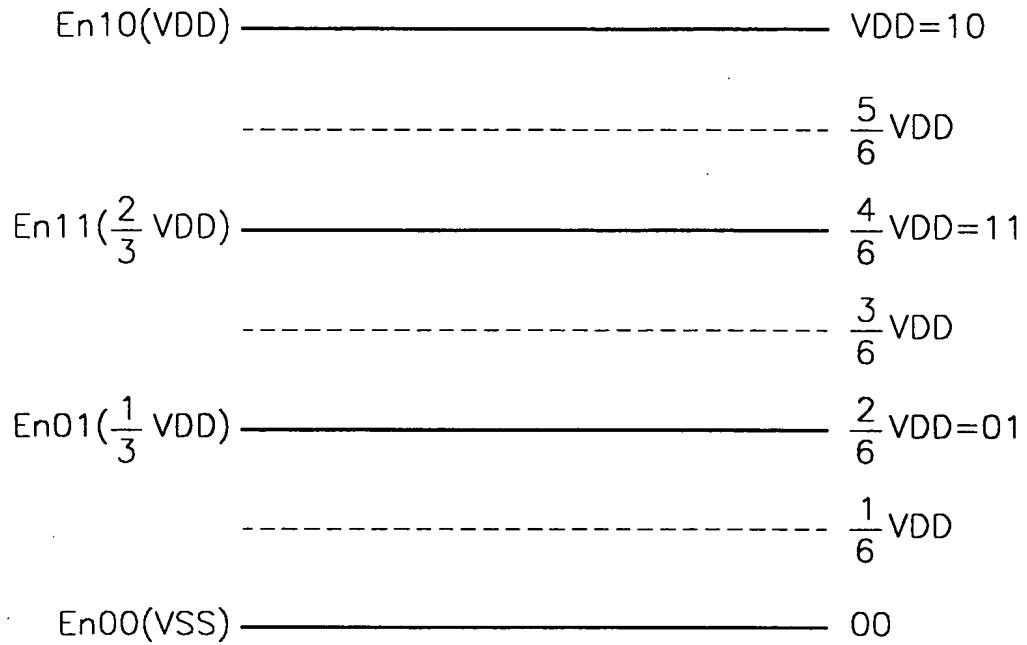


FIG. 1



**FIG. 2**



**FIG. 3**

RTXL LTXL	En10	En11	En01	En00
En10	10(VDD)	$\frac{5}{6}$ VDD	11( $\frac{4}{6}$ VDD)	$\frac{3}{6}$ VDD
En11	$\frac{5}{6}$ VDD	11( $\frac{4}{6}$ VDD)	$\frac{3}{6}$ VDD	01( $\frac{2}{6}$ VDD)
En01	11( $\frac{4}{6}$ VDD)	11( $\frac{3}{6}$ VDD)	01( $\frac{2}{6}$ VDD)	$\frac{1}{6}$ VDD
En00	$\frac{3}{6}$ VDD	01( $\frac{2}{6}$ VDD)	$\frac{1}{6}$ VDD	00(VSS)

**FIG. 4**

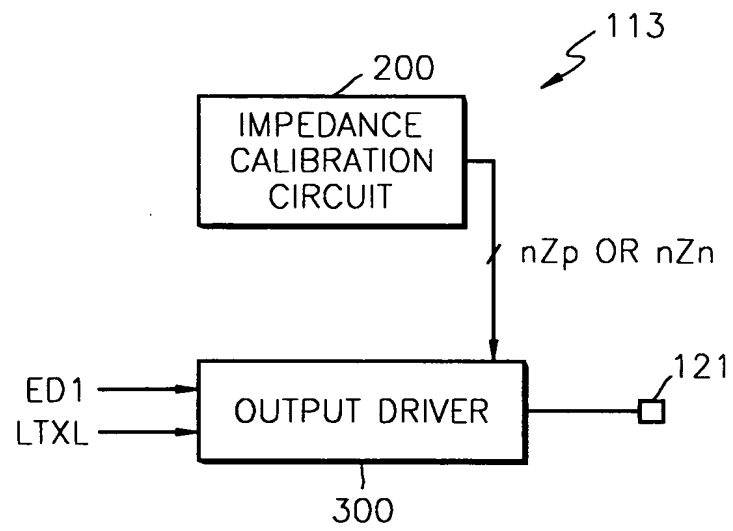


FIG. 5

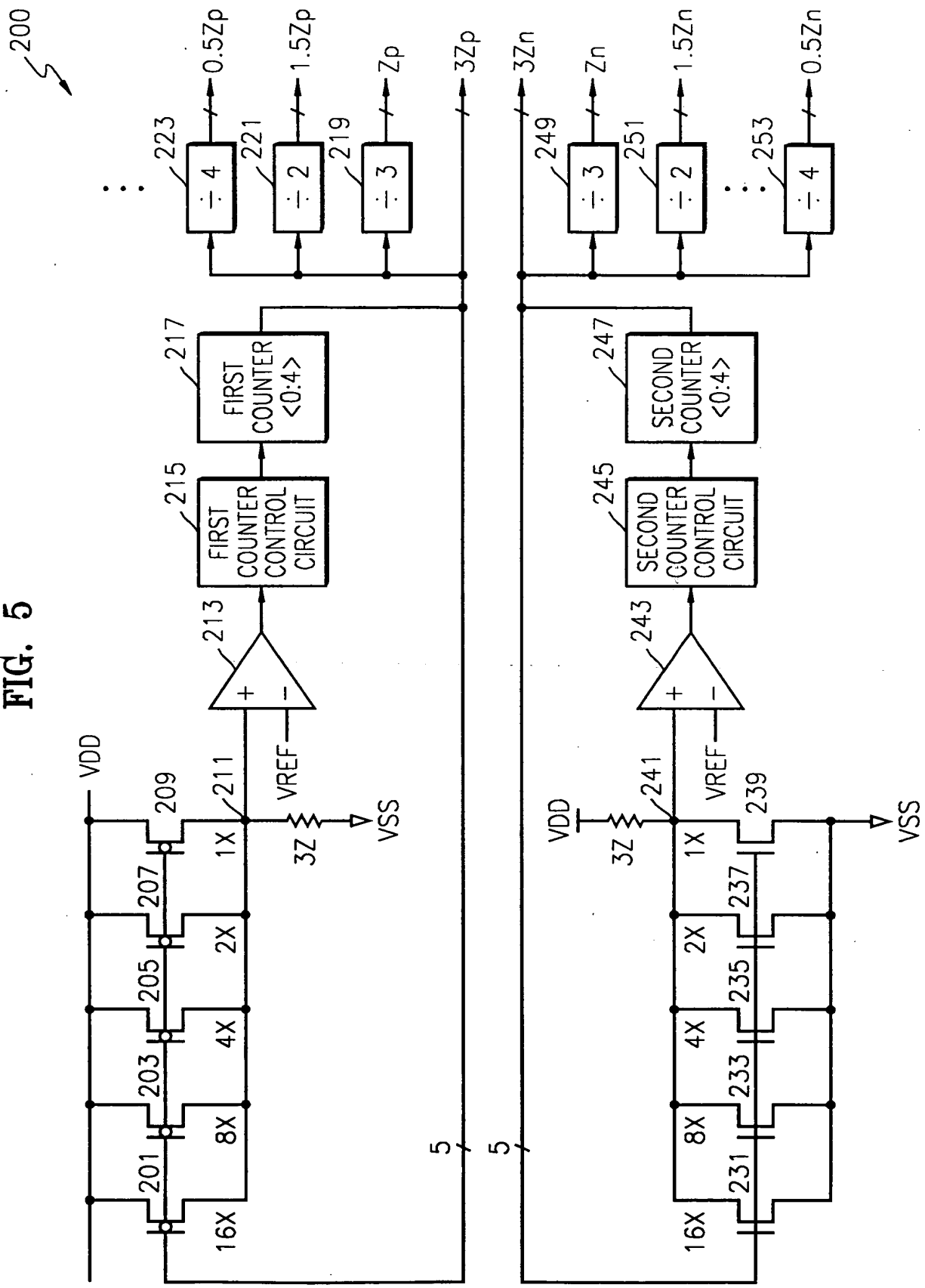


FIG. 6

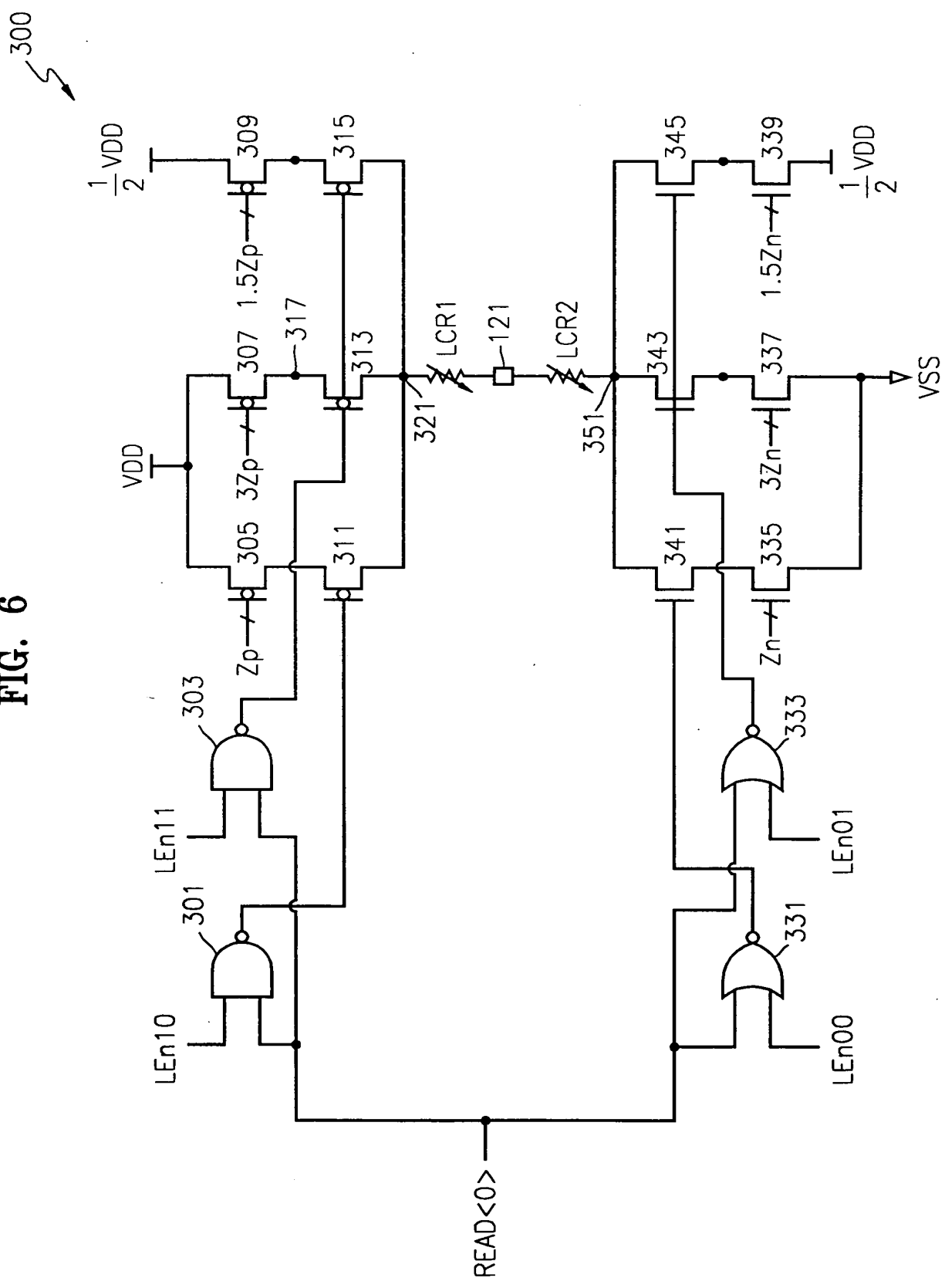


FIG. 7

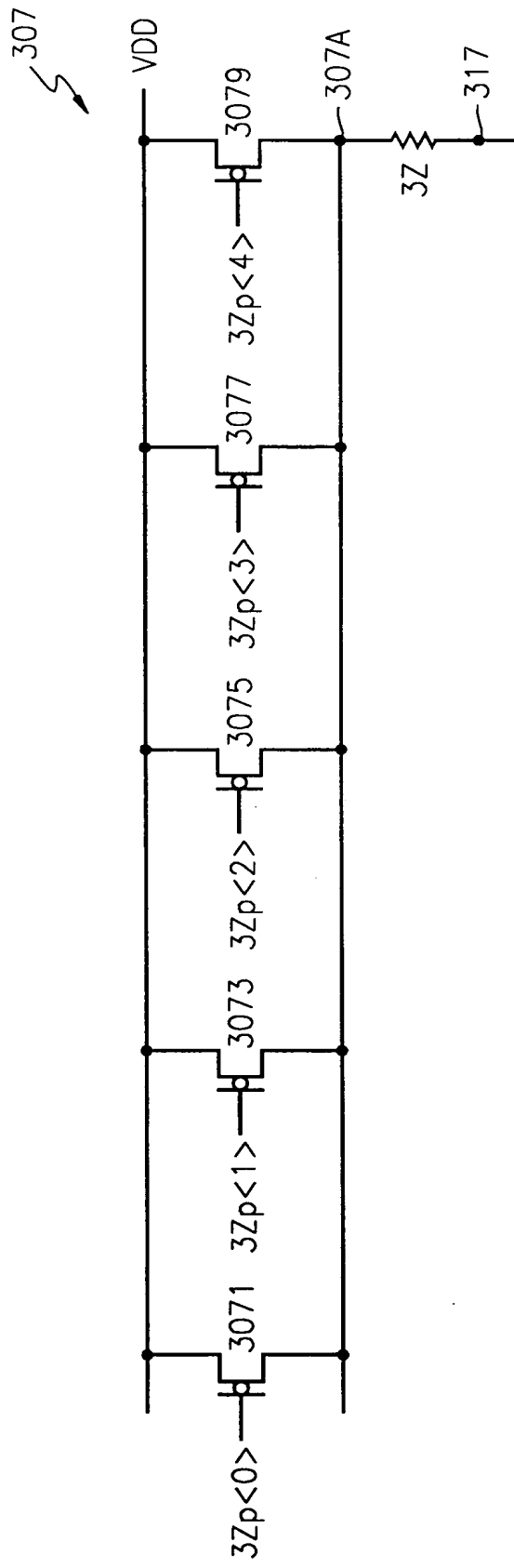


FIG. 8

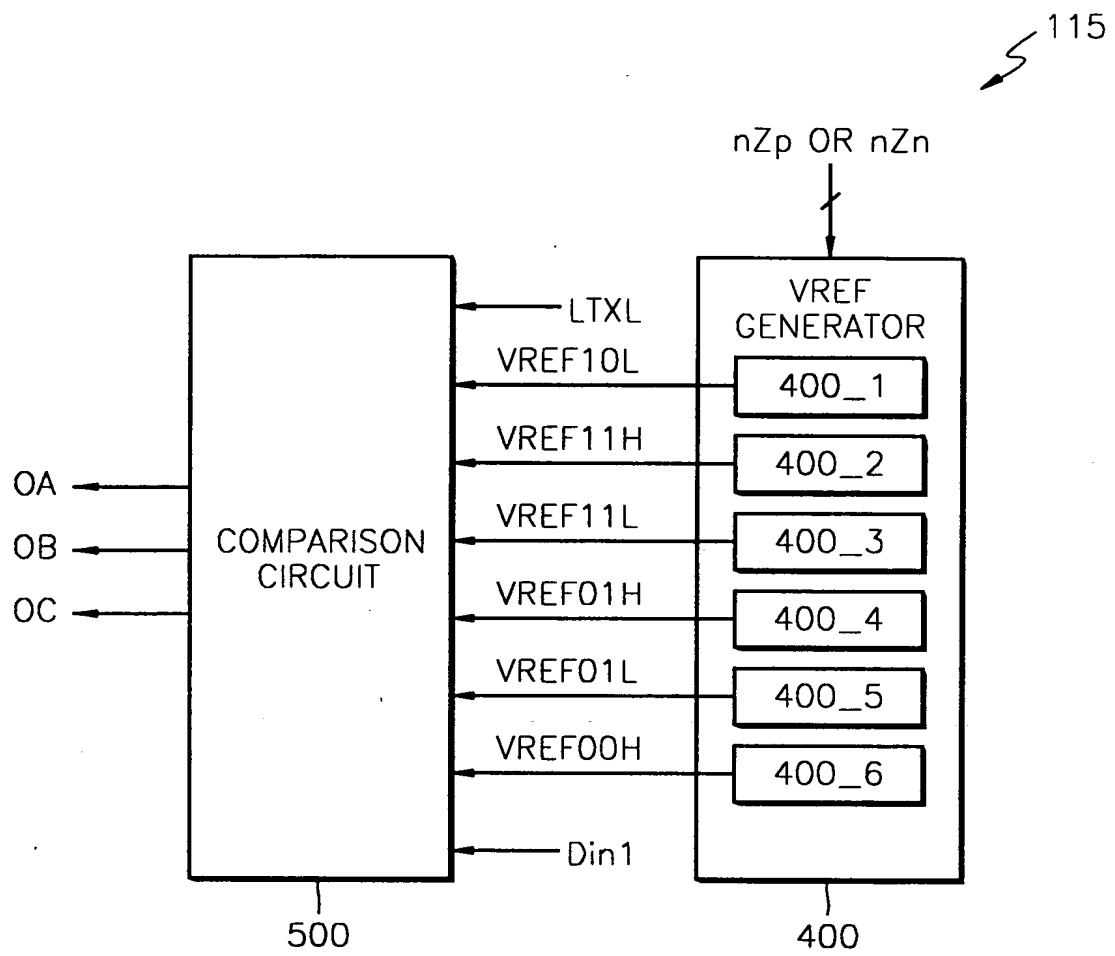


FIG. 9

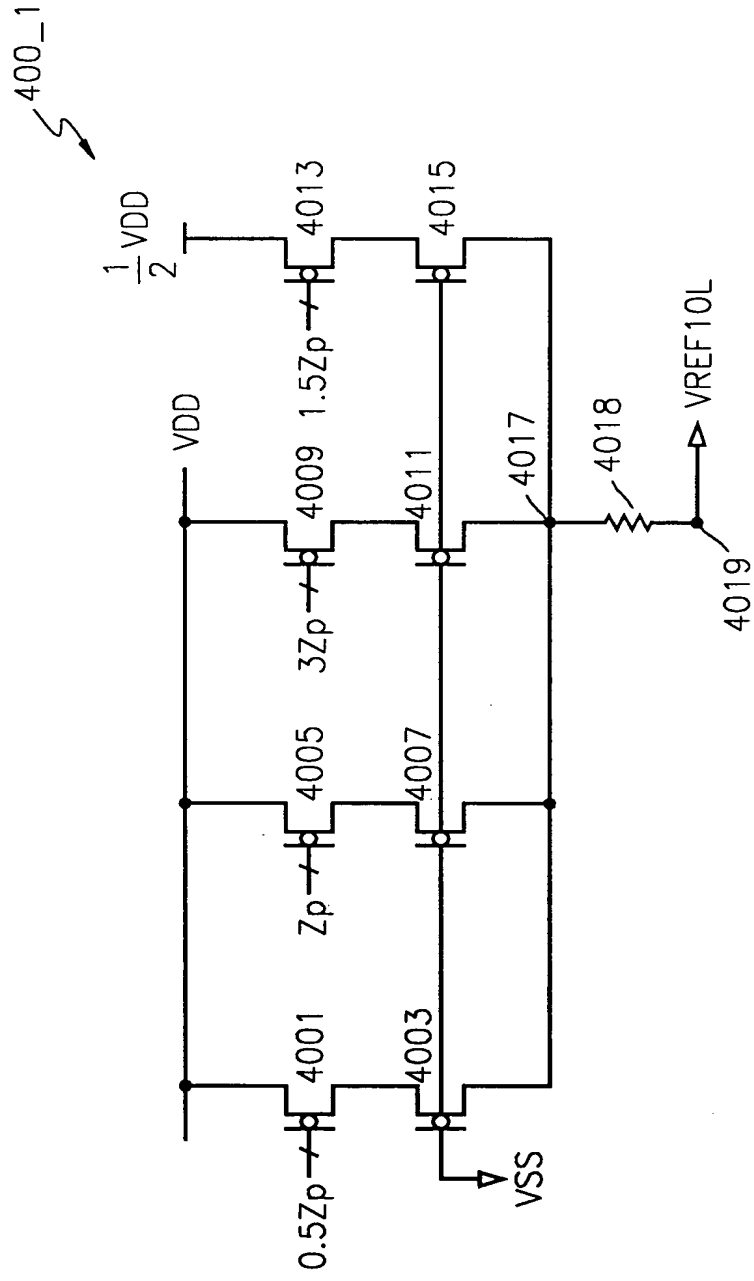




FIG. 10

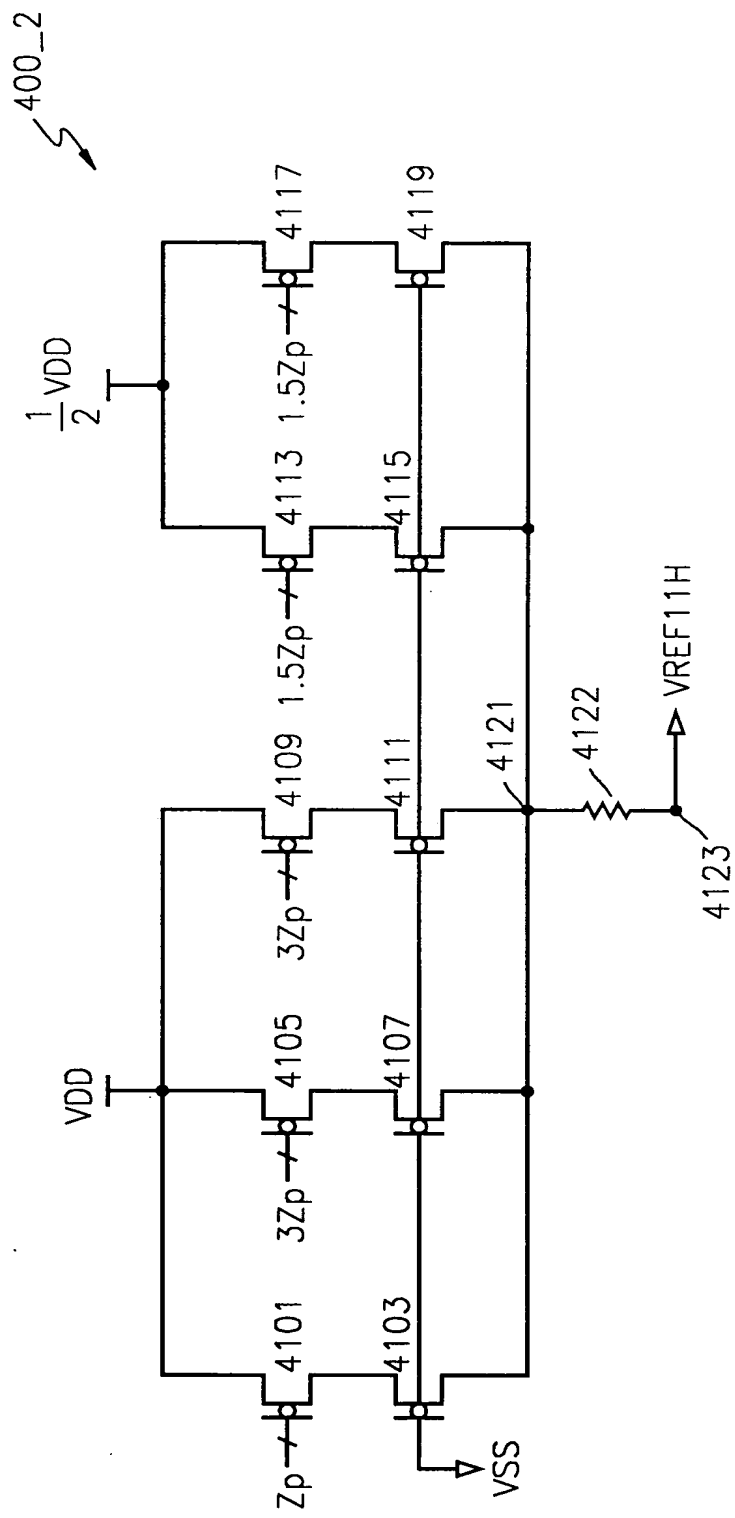


FIG. 11

400\_3

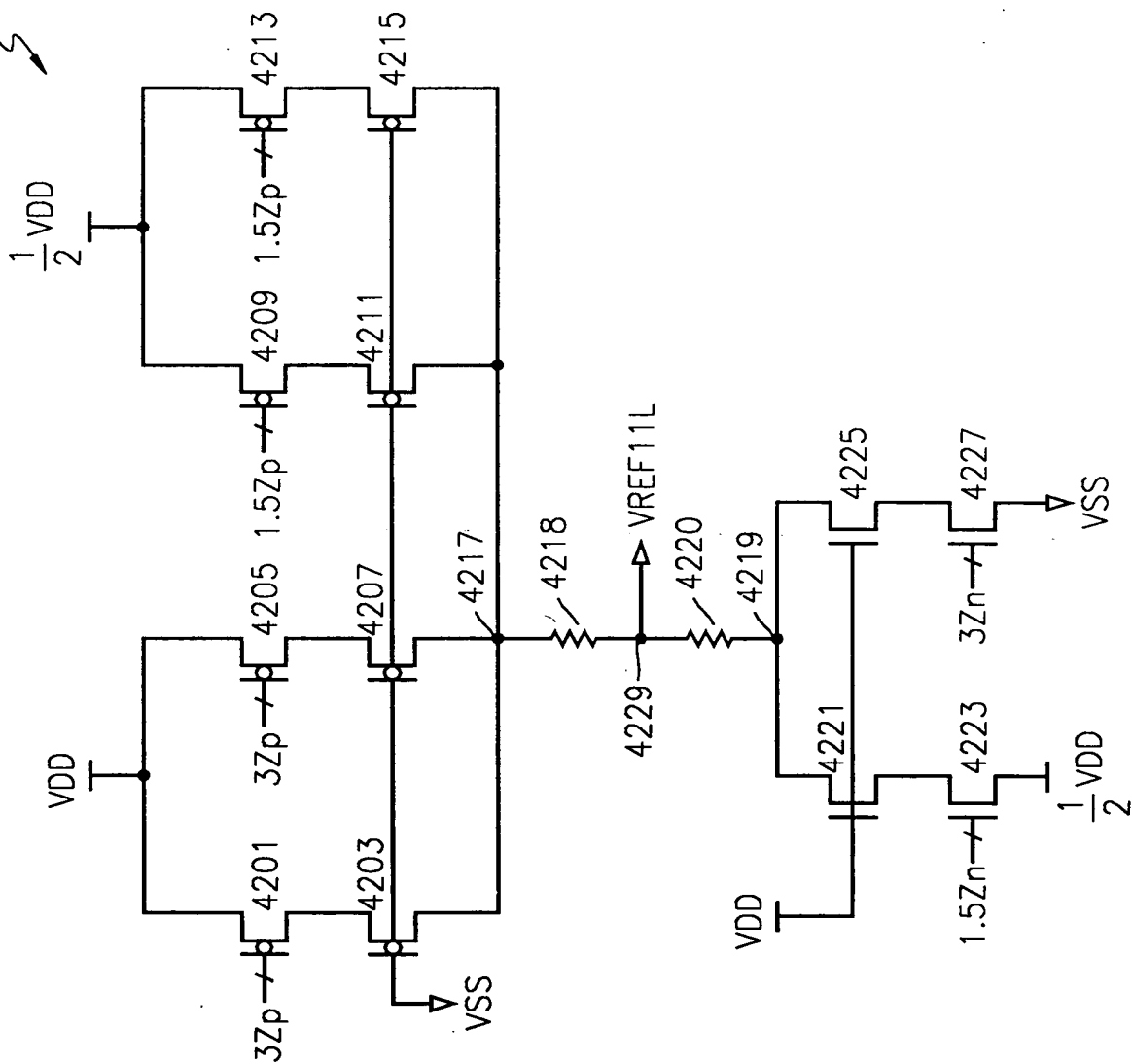


FIG. 12

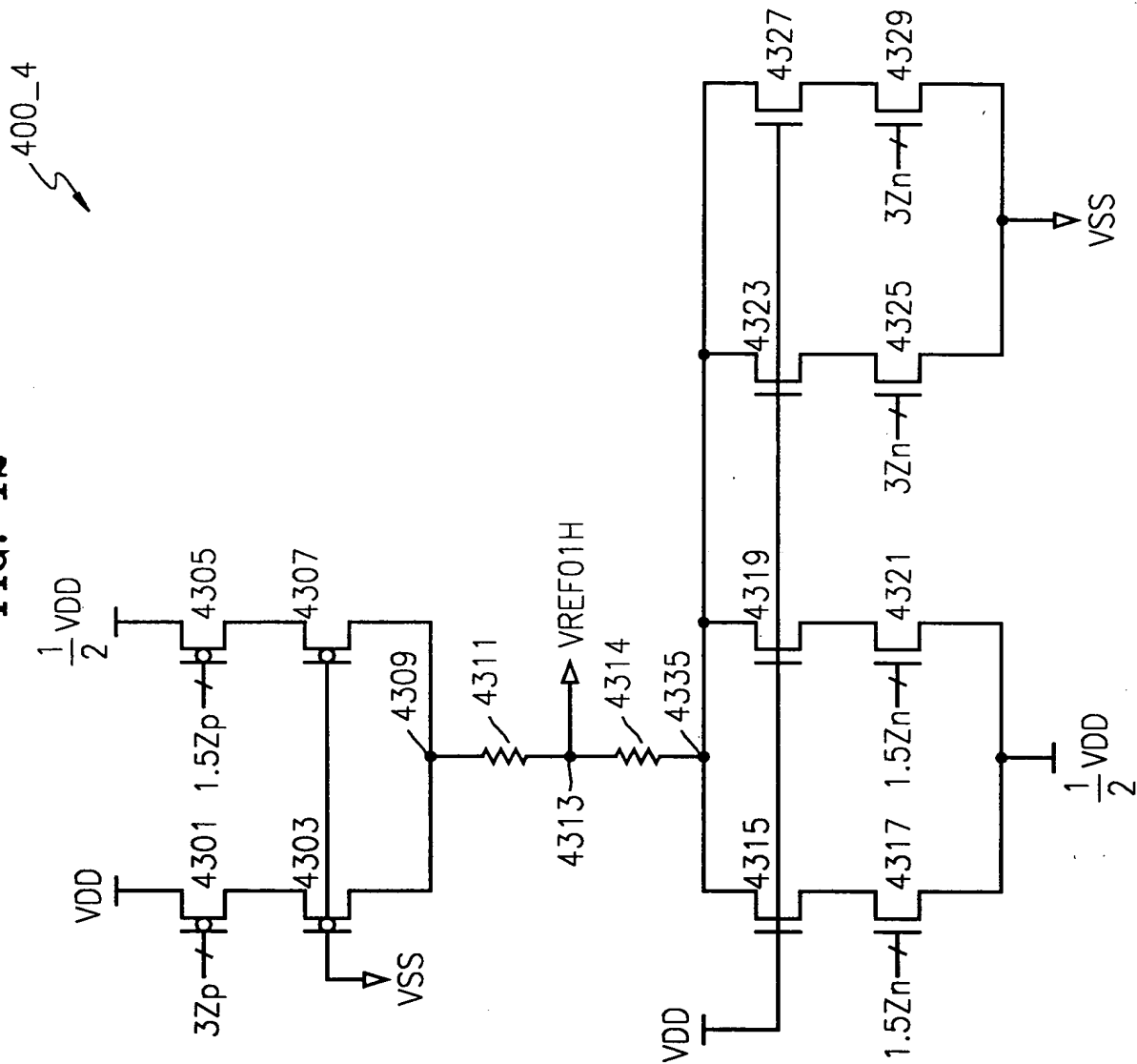
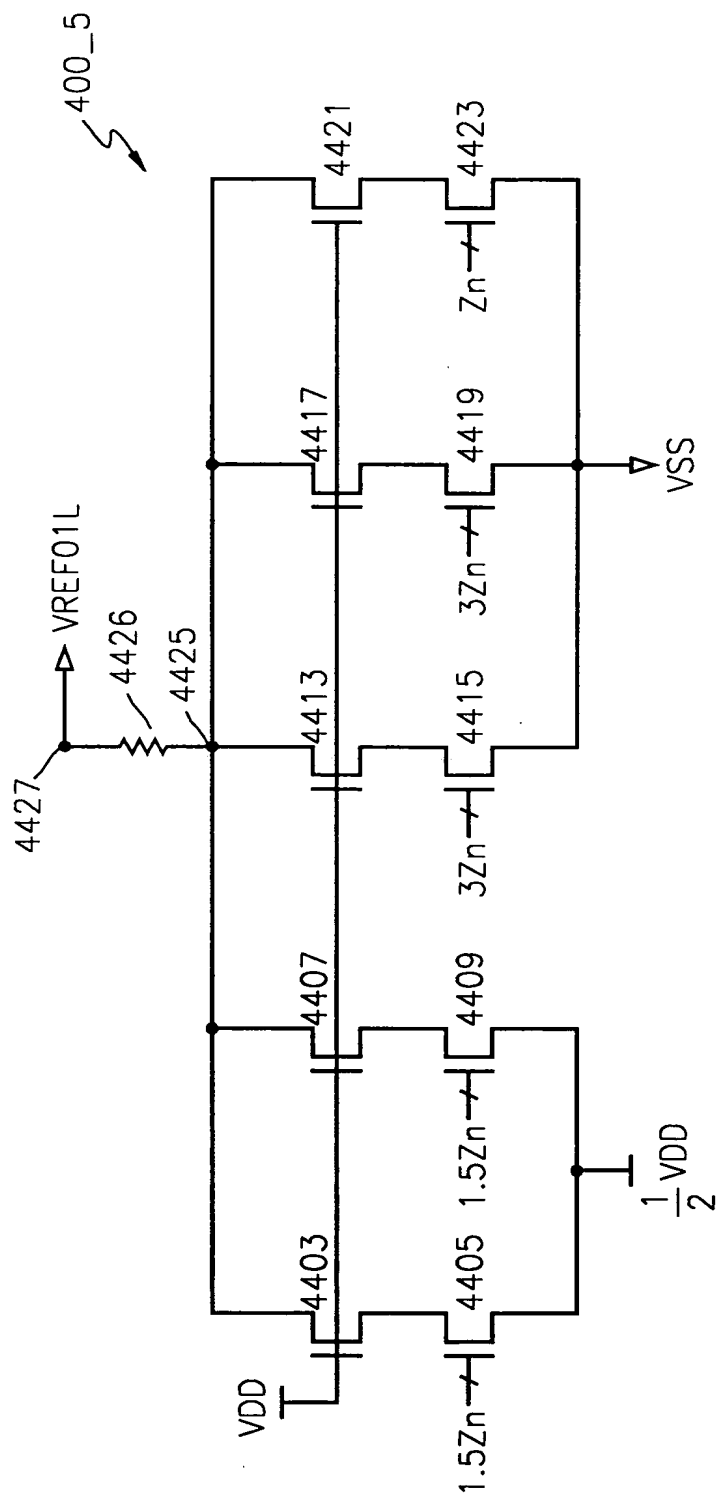


FIG. 13



**FIG. 14**

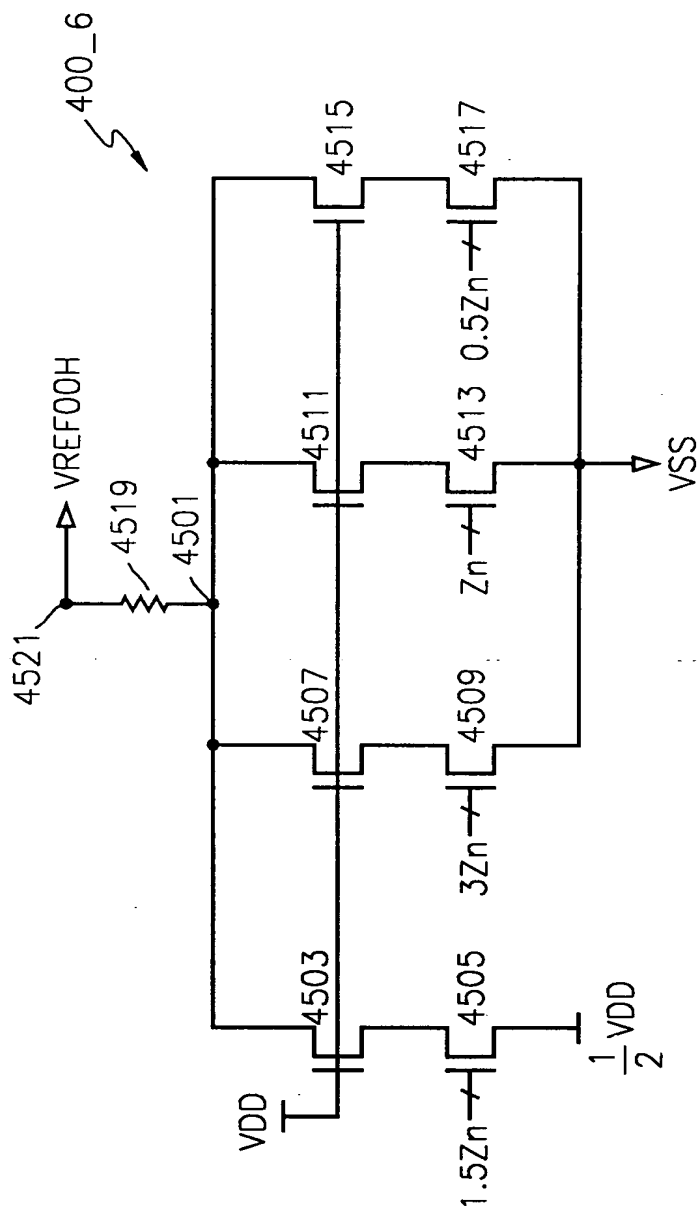


FIG. 15

VOLTAGE	CONDITIONS
10	10 ↔ 10
VREF10L	10 // (10 ↔ 11)
5/6VDD	10 ↔ 11
VREF11H	(10 ↔ 11) // {11v(10 ↔ 01)}
11	(11 ↔ 11)v(10 ↔ 01)
VREF11L	{11v(10 ↔ 01)} // {(11 ↔ 01)v(10 ↔ 00)}
3/6VDD	(11 ↔ 01)v(10 ↔ 00)
VREF01H	{(11 ↔ 01)v(10 ↔ 00)} // {01v(11 ↔ 00)}
01	(01 ↔ 01)v(11 ↔ 00)
VREF01L	{01v(11 ↔ 00)} // (01 ↔ 00)
1/6VDD	01 ↔ 00
VREF00H	(01 ↔ 00) // 00
00	00 ↔ 00

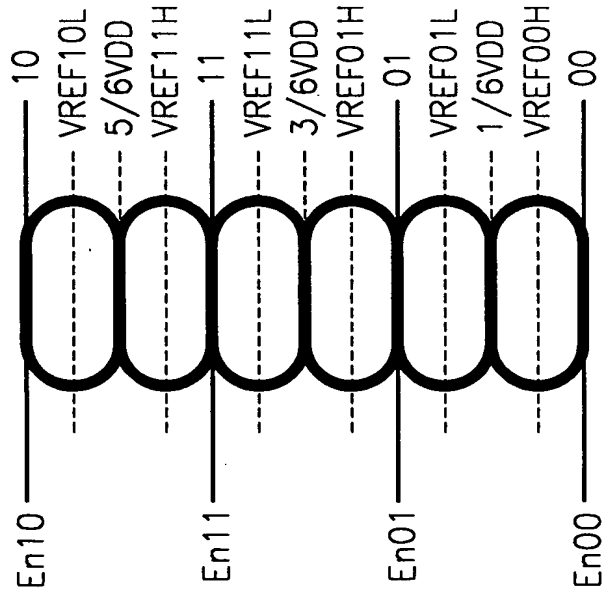
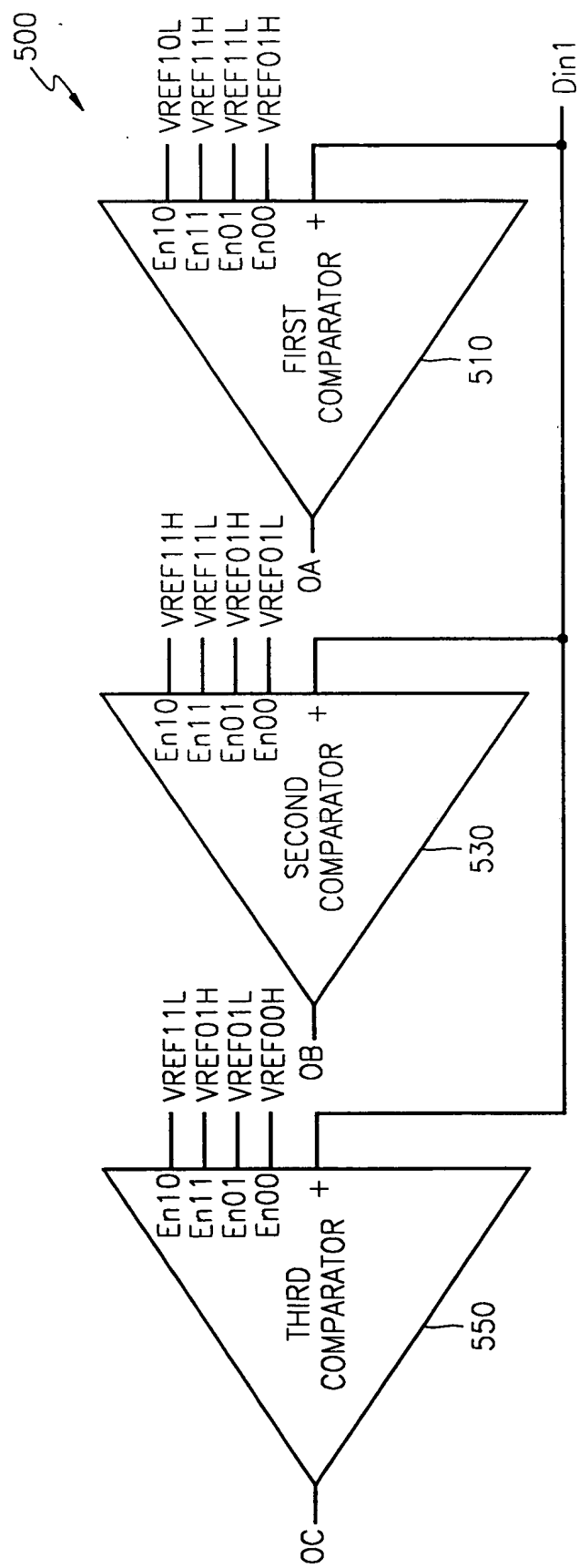


FIG. 16



**FIG. 17**

0A	0B	0C	ED2 (=ED1)	OD2 (=OD1)
H	H	H	1	0
L	H	H	1	1
L	L	H	0	1
L	L	L	0	0